EXHIBIT 1

UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

SOLAS OLED LTD., *Plaintiff,* v. LG DISPLAY CO., LTD., LG ELECTRONICS, INC., and SONY CORPORATION, *Defendants.*	Case No. 6:19-cv-00236-ADA

DECLARATION OF RICHARD A. FLASCK IN SUPPORT OF SOLAS'S OPENING CLAIM CONSTRUCTION BRIEF

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"a non-light emitting display voltage having a predetermined voltage value for allowing the optical element to perform a non-light emitting operation is generated as the gradation signal ('137 patent claim 39) **22**

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VIII. DISPUTED TERMS FOR '891 PATENT *30*

A. "a third thin film transistor which during driving its gate through a driving conductor taps a diode driving current at an output of said first current-driving transistor and supplies a current measuring- and voltage regulating circuit, said current measuring- and voltage regulating circuit providing to the data conductor a voltage signal which is dependent on a current measuring result and a voltage comparison" ('891 patent claims 10, 15, 36, 37, 39) **30**

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I, Richard A. Flasck, declare and state as follows:

I. INTRODUCTION

1. I have been retained as an expert in this case by Solas OLED Ltd. ("Solas"). I understand that Solas has asserted three patents in this case: U.S. Patent Nos. 7,907,137 ("'137 patent"), 7,432,891 ("'891 patent"), and 7,573,068 ("'068 patent"), (collectively "Asserted Patents").

2. I have been asked to consider and opine on claim constructions for disputed claims terms in these patents, which I set forth and address in separate sections below for each term.

3. In forming my opinions, I have reviewed, considered, and/or had access to the patent specifications and claims, their prosecution histories, the parties' proposed claim constructions, and the extrinsic evidence cited by the parties in connection with those proposed constructions. I have also relied on my professional and academic experience in the fields of flat panel, active-matrix, and/or LED displays. I reserve the right to consider additional materials as I become aware of them and to revise my opinions accordingly.

II. QUALIFICATIONS

4. My qualifications for forming the opinions set forth in this Declaration are summarized here and explained in more detail in my *curriculum vitae*, which is attached as Exhibit A.

5. I received a Bachelor of Science degree in Physics from the University of Michigan, Ann Arbor, in 1970. I thereafter received a Master of Science degree in Physics from Oakland University in Rochester, Michigan, in 1976. I am the founder and CEO of RAF Electronics Corp., where I developed and patented Liquid Crystal on Silicon (LCOS) microdisplay projection technology using active matrix transistor arrays as well as developed proprietary LED-based Solid State Lighting (SSL) products.

6. After receiving my bachelor's degree, I was employed as a scientist and a manager by Energy Conversion Devices, Inc., from 1970 through 1982. My work at Energy Conversion Devices concerned the development of electroluminescent displays, thin film photovoltaics, ablative imaging films, non-volatile memory, multi-chip modules, and superconducting materials. After leaving Energy Conversion Devices, I founded and served as CEO of Alphasil, Inc., where I developed amorphous silicon thin film transistor (TFT) active matrix liquid crystal displays (AMLCDs). My work at Alphasil included thin film transistor array substrate process and circuit design, data driver and gate driver design, scalers, video circuits, gamma correction circuits, backlighting, and inverter design. At Alphasil I also designed and incorporated touch panel screens into active matrix display devices. The touch panel technologies included surface acoustic wave and capacitive sensing. I worked at Alphasil from 1982 through 1989.

7. After leaving Alphasil, I founded RAF Electronics Corp., described above. I have served as CEO of RAF Electronics since that time. At RAF I developed HDTV projection technology including transistor array substrates for LCOS devices and the associated optical systems. My activities at RAF have included developments in lighting systems using both traditional LED and OLED (Organic Light Emitting Diode) technologies. In 2016 I was granted US Patent 9,328,898 which includes OLED and LED technology and lighting systems. In 2019 RAF received a CalSEED grant from the California Energy Commission to develop ultra-efficient lighting products and explore establishing a Central Valley manufacturing facility.

8. In 1997, I took the position of President and COO at Alien Technology Corporation, where I was responsible for completing a Defense Advanced Research Projects Agency (DARPA) contract, and for implementing MEM fluidic self-assembly (FSA) technology. I left that position in 1999.

9. In 2002, I co-founded and served as COO of Diablo Optics, Inc., where I developed, produced, and commercialized key optical components for HDTV projectors, such as polarization optics, condenser lenses, projection lenses, and ultra-high performance optical interference filters using thin film stacks in conjunction with LED and thin film transistor arrays and devices. I left Diablo in 2007.

10. I am listed as an inventor on twenty-six patents issued in the United States and foreign countries, including one United States design patent. My inventions concern technologies including LED devices, semiconductor materials, glass materials, non-volatile memory cells, thin film transistors, flat panel backplanes and displays, and wafer based active matrices, and various transistor array substrates.

11. I have authored or co-authored twenty-five articles or conference presentations, including numerous papers and presentations concerning lighting and display technologies. My curriculum vitae (Exhibit A) lists these articles, conference presentations, and patents.

12. I am also a member of several professional organizations, including the OSA, SPIE, AES, SID, and the IEEE.

13. In summary, I have almost 50 years of experience in the field of high tech product development including flat panel displays, transistor array substrates, touch panels, and OLED and LED devices.

14. In the past twelve years, I have served as an expert witness for patent infringement litigation (or arbitrations) or PTAB proceedings in the following cases:

- *Nichia Corporation v. Seoul Semiconductor*, 3:06-cv-0162 (NDCA), on behalf of Seoul Semiconductor Company, Inc.

- *Hewlett Packard v. Acer Incorporated et al.*, U. S. ITC Investigation No. 337-TA-606, on behalf of Acer Incorporated et al.
- *Samsung v. Sharp*, U. S. ITC Investigation No. 337-TA-631, on behalf of Samsung
- *Sharp v. Samsung*, U. S. ITC Investigation No. 337-TA-634, on behalf of Samsung
- *O2Micro v. Monolithic Power Systems et al.*, U. S. ITC Investigation No. 337-TA-666, on behalf of O2Micro
- IPR No. IPR2014-0168 of U.S. 7,612,843, on behalf of Petitioner Sony, Corp.
- *Ushijima v. Samsung*, 1:12-cv-00318-LY (WDTX), on behalf of Ushijima
- *Delaware Display Group LLC and Innovative Display Technologies LLC v. Sony Corp. et al.*, Case No. 1:13-cv-02111-UNA DDEL, on behalf of Sony Corp.
- *Funai v. Gold Charm Limited*, Case No. IPR2015-01468, on behalf of Petitioner Funai
- *Phoenix, LLC v. Exar et al.*, Case No. 6:15-CV-00436-JRG-KNM., on behalf of Exar et al.
- *MiiC v. Funai*, Case No. 14-804-RGA, on behalf of Funai
- *Delaware Display Group LLC v. Vizio*, Case No. 13-cv-02112-RGA, on behalf of Vizio
- ARRIS v. Sony, U.S. ITC Investigation No. 337-TA-1060, on behalf of Sony
- *BlueHouse Global, LTD. v Semiconductor Energy Laboratory Co. LTD.*, IPRs on behalf of BlueHouse Global, LTD
- *Phoenix, LLC v. Wistron Corp.*, Case No. 2:17-cv-00711-RWS, on behalf of Wistron Corp.
- *Ultravision v Absen et al*., ITC Investigation No. 337-TA-1114, on behalf of Absen et al.
- *Viavi Solutions Inc. v Materion Corp.*, PGR2019-00017, on behalf of Viavi Solutions, Inc.
- *NEC v Ultravision*, IPR2019-01123 and IPR2019-01117, on behalf of NEC
- *Solas OLED Ltd., v. Samsung Display Co., Ltd., et al.*, Case No. 2:19-cv-00152-JRG, on behalf of Solas

III. TECHNOLOGY BACKGROUND

21. Semiconductor devices are electronic components that exploit the electronic properties of semiconductor materials, such as silicon. Semiconductor materials are useful because their behavior can be easily manipulated by the addition of impurities, known as doping. Current conduction in a semiconductor occurs via mobile or "free" electrons and holes, collectively known as charge carriers. Doping a semiconductor such as silicon with a small proportion of an atomic impurity, such as phosphorus, greatly increases the number of free electrons or holes within the semiconductor (a doped semiconductor containing excess holes is called "p-type"; one containing excess free electrons is known as "n-type").

22. A thin film transistor, or TFT, is an example of a semiconductor device. TFTs can be used as simple ON/OFF switches in a wide variety of electrical devices, such as active-matrix LCD displays. Basically, a TFT consists of a semiconductor and three electrodes: (i) the gate electrode; (ii) the source electrode; and (iii) the drain electrode. The gate electrode must be insulated from the semiconductor by a dielectric layer (or gate insulation layer), while the drain electrode and source electrode must both directly contact the semiconductor. Because of this, TFTs generally have one of the following configurations:

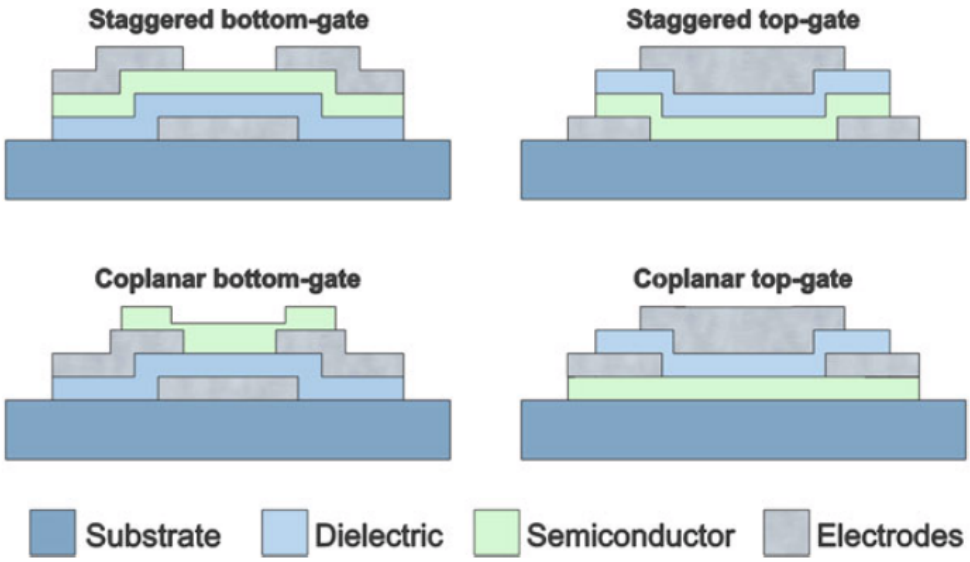


Fig. 2.2 The most typical TFT structures depending on the positioning of layers

where "coplanar" in the drawings above refers to the gate electrode being one the same side of the semiconductor as the source and drain electrode; "staggered" refers to the gate electrode being on the opposite side of the semiconductor; and "top" and "bottom" refer to the location of the gate electrode relative to the other layers.

23. In integrated circuit processing (e.g. TFT active matrix processing), when a vertical edge (or wall) must be made in two stacked layers, a single mask must be used once to pattern the edge. Mask registration and tolerances prevent the use of two masks (or even the same mask used twice) to form such structures. The bad practice of using two masks or using the same mask in two separate photolithographic exposures inevitably leads to a mismatch in edge placement in the two layers. This edge mismatch in turn will cause subsequent step coverage and etching problems. Such problems are ruinous to product yield.

24. Examining Fig 8 of the 068, or example, we see at least two cases where coincident vertical walls are shown. These two occurrences are marked by oval A and oval B.

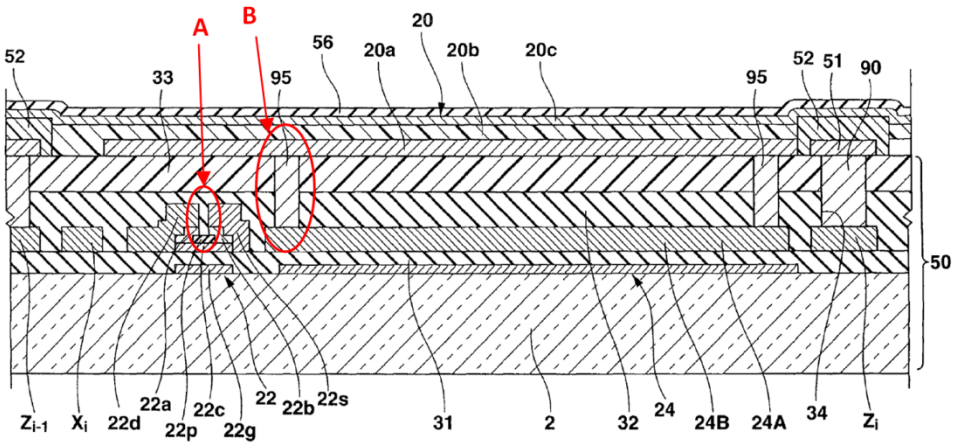


FIG.8

25. In oval A, we see a coincident vertical walls in ***22d*** (the drain) and ***22a*** (a doped semiconductor layer). We also see the vertical coincident vertical wall configuration in ***22s*** (the source) and ***22b*** (a doped semiconductor layer).

26. The patent teaches that the drain ***22d*** and source ***22s*** are part of the "drain layer." '068 col: 9:44-49 teaches "The conductive film as the base of the drains ***21d*** and sources ***21s*** of the switch transistors ***21*****,** the drains ***22d*** and sources ***22s*** of the holding transistors ***22*****,** the drains ***23d*** and sources ***23s*** of the driving transistors ***23*****,** the electrodes ***24A*** of the capacitors ***24*****,** the scan lines *X1* to *Xm,* and the supply lines *Z1* to *Zm* will be referred to as a drain layer hereinafter."

27. The patent teaches that the drain layer is patterned. '068 col: 9:50-53, " FIG. **10** is a plan view showing a state wherein the drain layer is patterned. FIG. **11** is a plan view showing a state wherein the patterned drain layer is superposed on the patterned gate layer."

28. Further, the patent teaches that the drain layer ***22d*** and the source layer ***22s*** can comprise more than one layer. As explained at '068 col 8 47-51 "The drain ***22d*** is formed on one impurity-doped semiconductor film ***22a.*** The source ***22s*** is formed on the other impurity-doped

semiconductor film ***22b.*** The drain ***22d*** and source ***22s*** can have either a single-layer structure or a layered structure including two or more layers."

29. Finally, the patent teaches that the patterning of the drain ***22d*** and source ***22s*** is done with the usual photolithography. At '068 col14:46-48teaches: "The drain layer is sequentially subjected to photolithography and etching to pattern the drains ***21d*****,** ***22d,*** and ***23d*****,** the sources ***21s*****,** ***22s*****,** and ***23s…*****"**

30. Electricity flows like water. For a linear element in the circuit, the quantities of Voltage (V), Current (I) and Resistance (R) are related. Ohm's law is I=V/R. The action is not unlike water flowing from your home through a garden hose when you are watering your garden.

31. The current (I) is the amount of flow per unit time. For water we use gallons per minute. For electricity we use Amperes or "Amps" which is coulombs per second. A coulomb signifies a certain quantity of charge, similar to a "dozen." A dozen, however, is only 12 of something. A coulomb is about 6,000,000,000,000,000,000 electrons. So the current (I) in amps is the number of coulombs of electrons (or holes) flowing through an element each second.

32. The voltage (V) is like the water pressure coming from your house. For water we use the pressure unit pounds per square inch. For electricity we use Volts; it is the potential energy per unit charge (measured in Joules per coulomb). The harder we push (V), generally the more flow (I) we get.

33. Resistance (R) is the resistance to flow. With water, the resistance comes from turbulent flow, viscosity, and friction between the water molecules and the pipe walls. With electricity, it comes from the material properties of the element in question and its dimensions. Electrical resistance is measured in ohms. I=V/R. A larger voltage (pressure) V creates a larger flow (current I). A larger R (resistance) lowers the flow (I) for any given applied voltage. In ordinary electronic

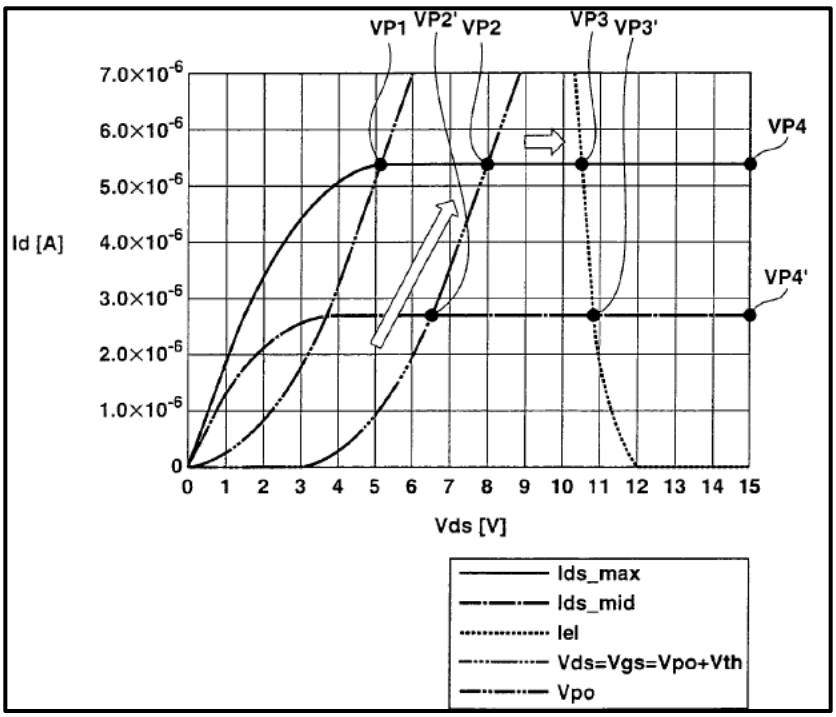
devices, e.g. not using superconducting devices, no current will flow without a voltage being applied, just as no water will flow from a hose without pressure. Similarly, some movement of charges, i.e. a current, is necessary in order to apply a voltage in an electronic circuit.

34. For our garden hose, the water pressure from the house is a given. When we turn on the spigot we get a certain flow. If the hose is kinked, additional resistance is introduced and the flow is reduced. On the other hand, with an unkinked hose, if the water company increases the water pressure, the flow increases.

35. Voltages and currents interact with each other in complex, but deterministic ways. Voltage and current are different entities, but are intrinsically inter-related. Ohm's law can be applied to linear electric elements, like resistors. Non-linear elements, like diodes and transistors, add additional aspects that must be considered.

36. A transistor (e.g. a thin film field effect transistor) is like a water spigot or gate valve. It can be turned fully off, partially on or fully on. The gate of a field effect transistor is like the handle on a water spigot. The level of voltage applied to the transistor gate regulates the current flow through the source/channel/drain of the transistor. There are threshold effects and saturation effects in transistors that produce their nonlinearity.

37. For example, below is the performance of a TFT shows the threshold voltage and nonlinear I-V characteristics, as described and taught in the '068 patent:



38. An electric circuit, like the pixel circuit of a OLED display is a combination of nonlinear and linear devices, which electronically interact with each other. OLED display panels are currently used in high-end mobile phones, watches, televisions, and other products from a number of manufacturers.

39. Displays used in phones, watches, televisions, etc. contain a two-dimensional array of picture elements, commonly called pixels, that can each be controlled to produce a desired color and brightness of light. Together, these pixels form the desired image on the display. Each pixel is typically made up of a number of sub-pixels, commonly in colors red, green, and blue, corresponding to the three primary colors visible to most human eyes. By controlling the brightness of each sub-pixel, the brightness and color of an overall pixel can be controlled.

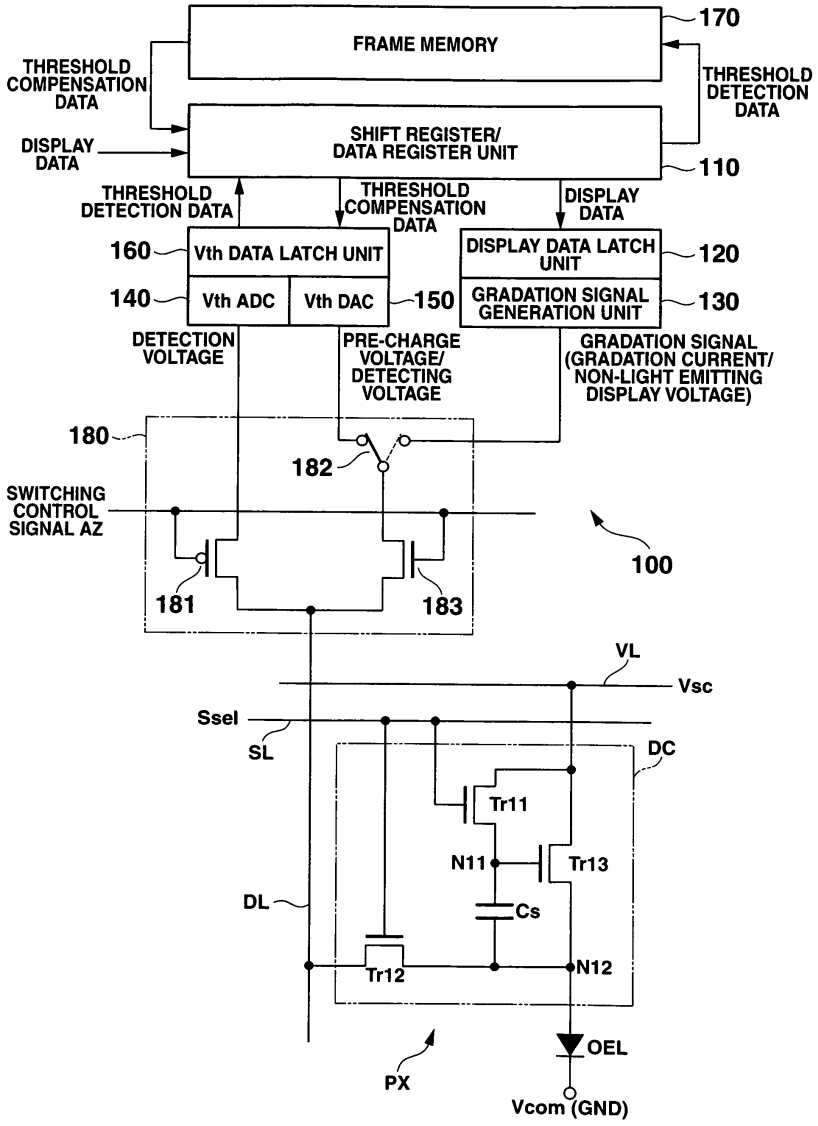
40. Unlike liquid crystal display technology, which uses a backlight, in OLED or other electroluminescent displays, each individual sub-pixel of the display directly emits light. OLEDs are current-controlled, meaning that the light emitted from each sub-pixel depends on the current that flows through the electroluminescent element in that sub-pixel. This means that each sub-pixel in the display has a circuit associated with it, commonly containing electronic components such as transistors and capacitors, which is responsible for sending the correct amount of current through the electroluminescent element and thus controlling the brightness of the sub-pixel.

III. BACKGROUND OF ASSERTED PATENTS

A. ’137 Patent

41. The ’137 patent concerns driving circuitry for self-luminous displays that emit light due to the current flowing through pixel elements, such as displays utilizing organic electroluminescent or LED elements. ’137 patent at 1:17–26, 36–43. The current flowing through such devices is commonly controlled by a gate voltage on a drive transistor. Id. at 3:15–30. However, the relationship between the gate voltage and the current may change “depending on the usage time, the drive history and the like,” and in particular the minimum “threshold voltage” on the gate necessary to permit current flow may shift. Id.

42. The ’137 patent provides structures and methods for driving the pixel circuits that solve problems in the prior art, including by detecting the threshold voltage for each pixel and applying a “compensation voltage” that compensates for such differences in such threshold voltages. Id. at 3:59–65.



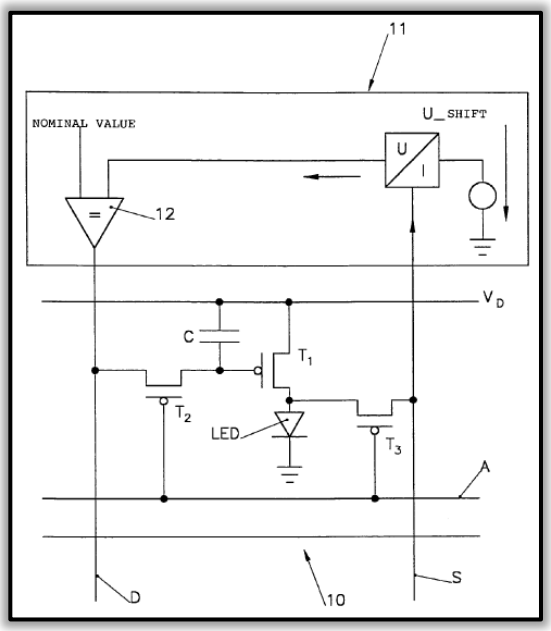
'137 patent, Fig. 1.

B. '891 Patent

43. The '891 patent concerns an active matrix drive circuit with current feedback for an organic light-emitting diode (OLED) image seen.'891 patent at Abstract, 1:5–61. The patent addresses a well-known problem with such circuits: "manufacturing-dependent fluctuations of the parameters of the thin film transistors" affect the amount of current provided to each OLED. *Id.* These differences may cause OLEDs to emit different amounts of light. *Id.*

44. Prior-art solutions used feedback to compensate for differences in drive transistors but used at least four transistors in the drive circuit, and/or drive circuit elements on both sides of the diode, making manufacturing difficult. *Id.* at 2:22–31, 2:45–53. The '891 patent solves the problem by disclosing a novel drive circuit that requires "only three thin film transistors" and a "current measuring and voltage regulating circuit" to compensate for any deviations. *Id.* at 2:9–31.

45. This drive circuit "avoids the disadvantages of the prior art" and "requires less components and is simpler to manufacture than the known circuits." *Id.* at 1:58–63. In particular, the OLED, due to its non-linear switching characteristics acts like a switch, so "no separate switch must be provided for the current." 2:19–26. This structure allows all circuit parts to be located at one side of the diode, "so that a conventional layer sequence can be used during manufacture." *Id*. Further, no contacts need to be guided through the organic material of the diode. *Id.* at 2:27–31.



C. ’068 Patent

46. The ’068 patent concerns improved designs for transistor array substrates, containing an array of “driving transistors” and associated lines and interconnections necessary to their operation. Such arrays of driving transistors are needed, for example, to drive active matrix displays utilizing organic electroluminescent elements. ’068 patent at 1:24–36.

47. In prior art arrays, the materials, dimension, and arrangement of the transistor components and the lines and interconnections meant that the arrays suffered from undesirably large resistances and voltage drops, impairing the operation of driving transistors and the quality of the displayed image. The ’068 patent teaches and claims improved designs for transistor arrays, with different arrangements of transistors, lines, interconnections, and electrodes, as well as with different dimensions or materials for such structures than those used in the prior art. E.g., ’068 patent, Fig. 5.

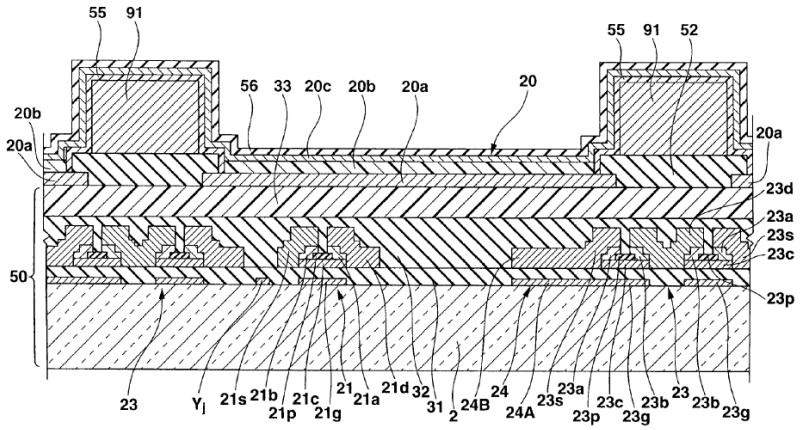


FIG.5

IV. LEVEL OF ORDINARY SKILL IN THE ART

48. In my opinion, a person of ordinary skill in the relevant art (“POSITA”) for the Asserted Patents would be a person with a bachelor’s degree in physics, electrical engineering, or a related field with approximately 3–5 years of experience in active-matrix and/or LED displays and systems, or a postgraduate degree such as a master’s degree in physics, electrical engineering, or a related field with approximately 1–2 years of experience in active-matrix and/or LED displays

and systems. A person with less education but more relevant practical experience, or vice versa, may also meet this standard.

49. I further note that I am at least a POSITA and that for 50 years I have worked with colleagues who are POSITAs. Thus, I am well qualified to give technical opinions from the perspective of a POSITA.

V. CLAIM CONSTRUCTION PRINCIPLES

50. I understand that a claim construction inquiry begins and ends in all cases with the actual words of the claim. Thus, quite apart from the written description and the prosecution history, the claims themselves provide substantial guidance as to the meaning of particular terms. I further understand that to begin with, the context in which a term is used in the asserted claim can be highly instructive. The patent specification can also shed light on the meaning of claim terms.

51. I understand that when conducting a claim construction inquiry, district courts are not (and should not be) required to construe every limitation present in a patent's asserted claims. Simply put, claim construction is not an obligatory exercise in redundancy. I further understand that where a term is used in accordance with its plain meaning, the court should not re-characterize it using different language.

52. I understand that there is a "heavy presumption" that claim terms carry their full ordinary and customary meaning, unless the accused infringer can show the patentee expressly relinquished claim scope. The ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention. Thus, the task of comprehending the claims often involves little more than the application of the widely accepted meaning of commonly understood words.

53. I understand that without clear and unambiguous disclaimer, courts do not import limitations into claims from examples or embodiments appearing only in a patent's written description, even when a specification describes very specific embodiments of the invention or even only a single embodiment. Similarly, statements during patent prosecution do not limit the claims unless the statement is a clear and unambiguous disavowal of claim scope.

54. I understand that Defendant bears the burden of proving that a claim is indefinite by clear and convincing evidence. I understand that a patent is invalid for indefiniteness if its claims, read in light of the specification delineating the patent, and the prosecution history, fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention.

VI. AGREED TERMS

55. I understand that Solas and Defendants LG Display Co., LTD., LG Electronics, Inc., and Sony Corporation (collectively, "Defendants") have agreed to the following constructions:

- "luminance gradation" ('137 patent claims 10, 36) means "light emitting level"
- "supply lines" ('068 patent claims 1, 13) means "conductive lines supplying current or voltage"

VII. DISPUTED TERMS FOR '137 PATENT

A. "a gradation current having a current value" ('137 patent claims 10, 36)

Solas's Proposed Construction	Defendants' Proposed Construction
"gradation current" means "current conveying information about a level"; thus, the full construction is a current having a current value and conveying information about a level	an actual current (not voltage) with a value corresponding to a luminance level

56. The parties appear to be in agreement that a "gradation current" must be a current. They also do not appear to dispute what the phrase "having a current value" means.

57. Solas's proposal explains that the gradation current "convey[s] information about a level." This matches the purpose of the gradation current in the larger claim element: "a gradation current having a current value for allowing the optical element to perform a light emitting operation at a luminance corresponding to a luminance gradation of display data." ('137 patent at 58:5–8, 62:55–59.)

58. Defendants' proposal instead says that the gradation current "correspond[s] to a luminance level." It appears to me that this language simply repeats the claim surrounding claim language "corresponding to a luminance gradation" and the parties agreed construction for "luminance gradient" of "light emitting level." Solas's language actually explains what the "gradation current" is, rather than parroting other claim limitations, and in my opinion it should be adopted.

59. The central difference between the proposals is that Defendants replace the word "current" with "actual current (not voltage)." Defendants do not attempt to explain or define what a current is. That presumably is because a POSITA obviously would have no problem understand the scope of that well know term.

60. I have found nothing in the intrinsic record that distinguishes "actual" current from any other kind of current, and it is unclear to me how a juror would the "actual" currents from all of the other currents in the world that are not "actual."

61. I have also found nothing in the intrinsic record that supports excluding embodiments that otherwise satisfy the "gradation current" limitations, simply because those embodiments also involve a voltage. In fact, a POSITA would understand that adopting Defendants' proposed

construction would exclude embodiments. For instance, Figure 9 shows an embodiment while the "gradation current *Idata*" is flowing:

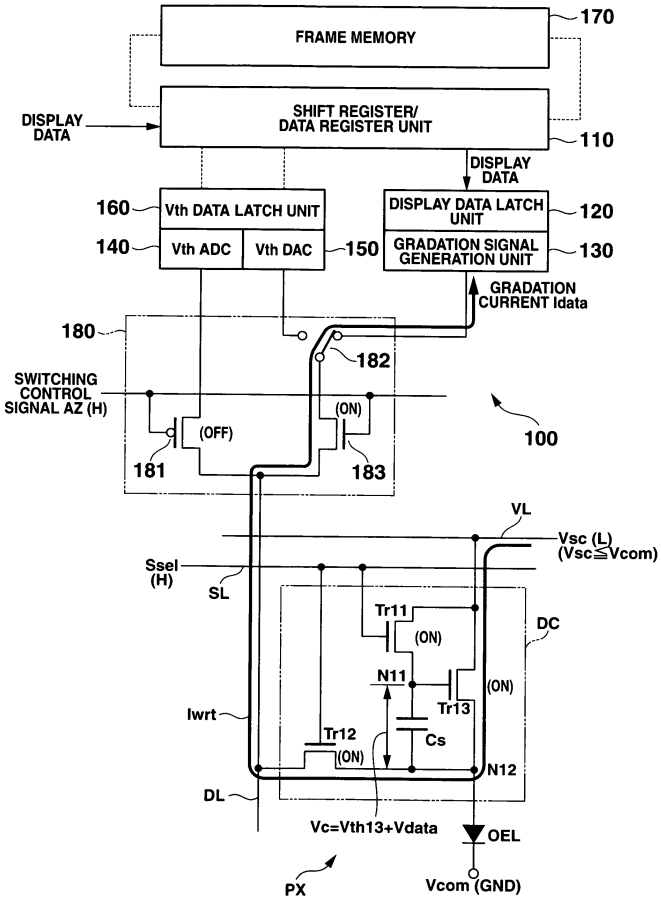


FIG.9

62. In this figure, each of elements 182, 183, and Tr12 act as switches ('137 patent at 12:52, 22:7–8), and as shown in Figure 9 each is "on," directly connecting the "gradation signal generation unit" 130 via "drive line" DL to contact point N12 within the "drive circuit" DC. As the specification explains, "the gradation current Idata is drawn via the data line DL, *whereby a voltage . . . is applied to the side of the source terminal* (the contact point N12 . . . ." (*Id.* at 22:20:25.) In other words, when the gradation current flows, the gradation signal generation unit

in this preferred embodiment supplies *both a current and a voltage* to the display pixel through the data line.

63. Claim 10 requires that the gradation signal generation circuit "generates a gradation current" and "supplies the gradation current." ('137 patent at 58:5–6, 10–11.) Under Defendants' proposal, the gradation signal generation circuit would need to generate and supply a "current (not voltage)." In my opinion, this improperly excludes the "gradation signal generation unit" of the preferred embodiments which generates and supplies both current and voltage.

64. There are further ways in which Defendants' proposal risks excluding preferred embodiments. The same preferred embodiment shown in Figure 9 can also operate in a "Non-Light Emitting Operation" phase where it also "suppl[ies] a non-light emitting display voltage Vzero." ('137 patent at 25:55, 27:3–15.) If Defendants' proposal prohibits the gradation signal generation circuit from ever supplying a voltage, the preferred embodiments are excluded for this reason, as well. I have been unable to identify any lexicography that suggests narrowing this term in this way. And Defendants have not pointed to—and I have been unable to identify—any clear disclaimer that supports Defendants' proposal either.

65. In addition, a POSITA would understand that the purpose of the gradation current in the preferred embodiments is to provide an appropriate "gradation voltage" that is applied to the gate of the drive transistor and directly controls the light emitted by the pixel. ('137 patent at 2:49–52, 11:4–13.) In the preferred embodiment, the gradation current supplies the electric charges to charge a capacitor with "the voltage component Vdata appropriately corresponding to the gradation signal (display data)." ('137 patent at 22:37–54.) The patent describes this latter process as "a current/voltage conversion function." (*Id.* at 24:38–39.) Moreover, the gradation current itself

was initially generated by converting a digital signal to an analog voltage and then applying a "voltage-current converter." (*Id.* at 10:60–11:3.)

66. A POSITA would understand this closeness of the inextricably intertwined relationship between voltage and current as well:

> Microsoft Computer Dictionary at 125 ("current: *n.* The flow of electric charge through a conductor, or the amount of such flow. Current is measured in amperes. *See also* ampere, coulomb. *Compare* volt.").
>
> Microsoft Computer Dictionary 3rd ed. (1997) at 502 ("volt: *n.* The unit used to measure potential difference or electromotive force. One volt is defined as the potential across which 1 coulomb of charge will do 1 joule of work, or the potential generated by 1 ampere or current flowing through 1 ohm of resistance *See also* electromotive force.").
>
> Microsoft Computer Dictionary at 502 ("voltage *n. See* electromotive force.").
>
> Microsoft Computer Dictionary at 172 ("electromotive force *n. The force that causes movement in charge carriers (the electrons) in a conductor*. Also called potential, voltage. *See also* ampere, coulomb.").

B. "gradation signal" ('137 patent claims 10, 15, 36, 37, 39)

Solas's Proposed Construction	Defendants' Proposed Construction
signal conveying information about a level	a gradation current with a current value sent to a pixel to set a luminance gradation

67. Based on their agreement on the meaning of "gradation luminescence," the parties appear to agree on the meaning of gradation; it infers "a level."

68. Solas's proposal properly explains the plain meaning of this term, in the context of the patent and claims in which is appears. The claim explains that the gradation signal "correspond[s]

to the luminance gradation of the display data" ('137 patent at 58:9–10), and the parties agree that a "luminance gradient" is a "light emitting level."

69. In my opinion, the Defendants' proposal is unhelpful. It repeats requirements that appear elsewhere in the claims such as the requirement that the "gradation current" be "supplie[d] . . . to the display pixel" or that it be related to the "luminance gradation." ('137 patent at 58:9–12.)

70. There is nothing in the plain meaning of "signal" that requires such an importation. The term "signal" is generally understand by a POSITA to convey any electrical quantity, such as voltage, current or frequency, that can be used to transit information." Microsoft Computer Dictionary at 435. And again, based on their agreement on the meaning of "gradation luminescence," the parties appear to agree on the meaning of gradation; it infer "a level."

71. While it is true that the claims require generating and/or supplying "a gradation current . . . as a gradation signal" ('137 patent 58:5–12, 62:55–60.), that does not mean that a "gradation signal" as the term is used in the '137 patent *must be* a gradation current. If anything, this claim language suggests the opposite, because if a "gradation signal" is necessarily also a "gradation current," there would be no reason to use both terms in the same claims. I have identified no lexicography that requires this narrowing from the plain meaning. And Defendants have not pointed to—and I do not see—any clear disclaimer that supports Defendants' proposal either.

72. The specification actually contradicts the attempted claim-term change present in Defendants' proposal. For example, Figure 1 of the patent has the label "gradation signal (gradation current / non-light emitting display voltage)." The specification has about one dozen other references to the "non-light emitting display voltage" as a "gradation signal." ('137 patent at 4:31–32, 5:38–39, 7:55–56, 10:47–52, 12:11–12, 13:2–4, 26:12–14, 29:57–58, 30:19–20, 31:29–30, 34:54–55, 36:23–25, 39:55–57, 46:25–26, 48:27–28, 51:25–26.)

73. And in my opinion the intrinsic record show no clear lexicography or disclaimer from the patentee that demonstrates the opposite.

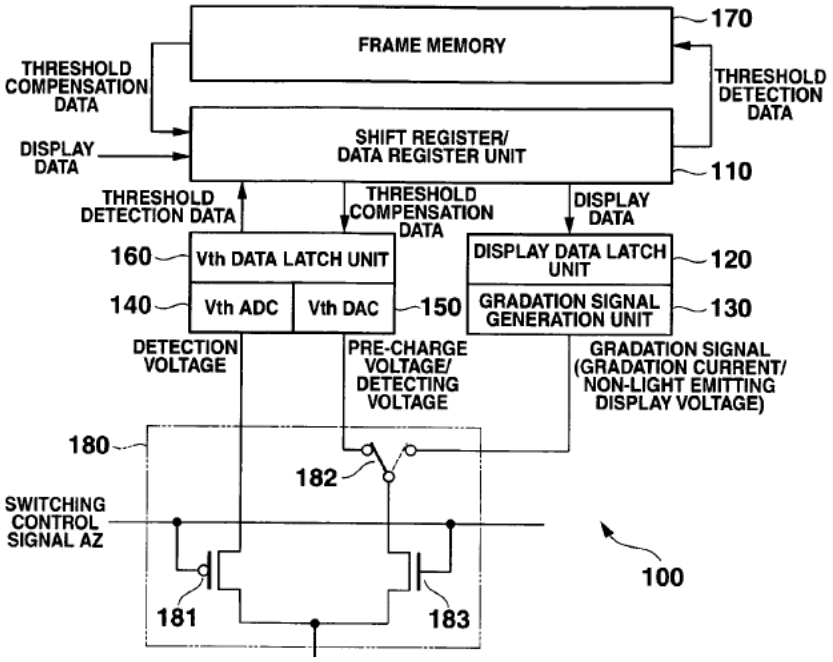
C. "generates, as the gradation signal, a non-light emitting display voltage having a predetermined voltage value" ('137 patent claim 15)

"a non-light emitting display voltage having a predetermined voltage value for allowing the optical element to perform a non-light emitting operation is generated as the gradation signal ('137 patent claim 39)

Solas's Proposed Construction	Defendants' Proposed Construction
Not indefinite	indefinite

74. It appears that, in Defendants' view, because the "gradation signal" must be a "gradation *current*" in the independent claims, then it cannot be a "non-light emitting display *voltage*" in the dependent claims.

75. Defendants' contention contradicts the clear teachings of the patent specification. In those teachings, the specification makes clear that the "gradation signal generation circuit can generate a "gradation current" and a "non-light emitting display voltage." Indeed, Figure 1 below (depicted below) makes this much clear visually:



76. Adding to this obvious point made by Figure 1, the specification includes about a dozen instances in which it makes clear that the "gradation signal generation circuit" provides signals—and that those signals convey the "gradation current" for a "light-emitting operation" and a voltage for a "non-light emitting operation." This much is clear in the "Summary of the Invention" section alone:

> The optical element preferably comprises a light emitting element which performs a light emitting operation at a luminance corresponding to a current value of a current applied. The operation of holding the voltage component based on the gradation signal includes: in the case where the light emitting element of said each display element is allowed to perform a light emitting operation at a luminance corresponding to a gradation luminance of display data, **generating, as the gradation current, a gradation current having a current value for allowing the optical element to perform a light emitting operation** at a luminance corresponding to the gradation luminance of the display data, and supplying the gradation current to the display pixel; and in the case where the light emitting element of said each display pixel is allowed **to perform a non-light emitting operation, generating, as the gradation signal, a non-light emitting display voltage having a predetermined voltage** for allowing the optical element to perform a non-light emitting operation, and supply the non-light emitting display voltage to the display pixel.

Various section of the Detailed Description reiterate this point and elaborate further on it, in various embodiments:

> As a consequence, compared with the case in which at the time of the non-light emitting operation, a gradation current corresponding to the non-light emitting display data is supplied via the data line DL to discharge substantially all the electric charges accumulated in the capacitor Cs connected between the gate and the source of the drive transistor Tr**13**, it is possible to favorably realize the non-light emitting state (the non-light emitting display operation) of the organic EL element OEL while shortening the time required for the writing operation of the non-light emitting display data. Accordingly, in addition to a display drive operation of performing the normal gradation display, a display drive operation of performing non-light emitting display is switched and controlled in accordance with the display data (the luminance gradation data) with the result that a light emitting operation having a desired number of gradations (for example, 256 gradations) can be clearly realized at a relatively high luminance.

Figure 34 illustrates the same concept, if there were any remaining shred of doubt:

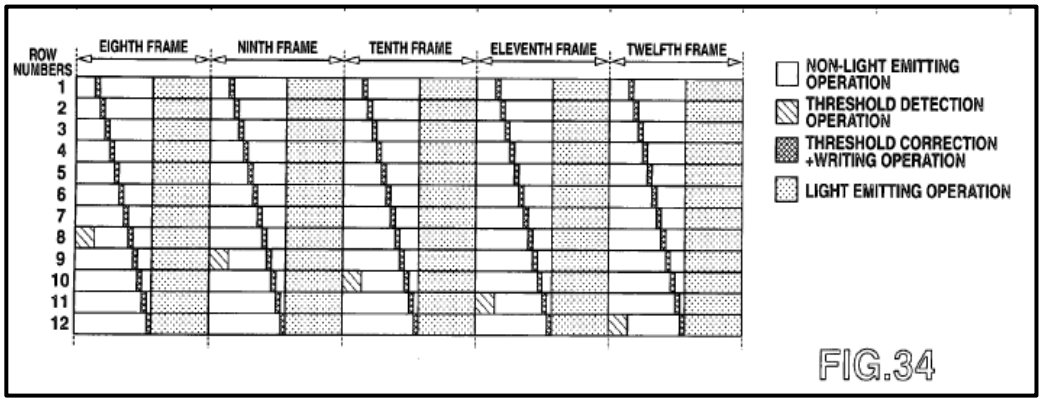


FIG.34

77. On and on the specification goes. In total, the specification has about one dozen other references to the "non-light emitting display voltage" as a "gradation signal." ('137 patent at 4:31–32, 5:38–39, 7:55–56, 10:47–52, 12:11–12, 13:2–4, 26:12–14, 29:57–58, 30:19–20, 31:29–30, 34:54–55, 36:23–25, 39:55–57, 46:25–26, 48:27–28, 51:25–26.)

78. Thus, any argument that the "gradation signal generation circuit cannot issue signals that both provide a gradation current and provide a non-light emitting display voltage is plain wrong.

79. Any reasonable reading of the claims themselves proves there is no tension between the dependent and independent claims. Rather, the claims are fully consistent with all these intrinsic-record teachings. For example, independent claims10 introduces the first aspect of the signals generated by the gradation circuit for a "light-emitting operation:"

> **a gradation signal generation circuit which generates a gradation current having a current value for allowing the optical element to perform a light emitting operation** at a luminance corresponding to a luminance gradation of the display data, **as a gradation signal** corresponding to the luminance gradation of the display data…

Perfectly consistent with the intrinsic record, Dependent claim 15 then introduces the second aspect, for the "non-light emitting operation":

> wherein the gradation signal generation circuit includes a circuit which generates, **as the gradation signal, a non-light emitting display voltage having a predetermined voltage value for allowing the optical element to perform a non-light emitting operation**.

80. Defendants' arguments also defy scientific principles underlying fundamental concepts in this patent. That is: any gradation signal would have a current component and some voltage value—and the two items are inextricably and mathematically intertwined. Indeed, due to this relationship, in ideal circuits, if you have one value, *you could solve for the other.* Thus, there is no basis for Defendants false premise that current can give no indication of voltage and voltage should give no indication of current. There is no lexicography that compels such extreme narrowing from the plain meaning. And Defendants have not pointed to—and cannot point to—any clear disclaimer of its invention from the prior art to warrant the narrowing it seeks, either.

81. In short, a POSITA would immediately understand the scope of these dependent claims. They are not indefinite.

D. ". . . through a data line . . . through the data line . . . through the data line"" ('137 patent claims 10, 16)

Solas's Proposed Construction	Defendants' Proposed Construction
plain and ordinary meaning. "a data line" means "one or more data lines." The antecedent basis for "the data line" is "a data line."	the gradation current is supplied, the threshold voltage is detected, and the compensation voltage is applied through the same data line

82. Defendants do not propose an actual construction for this term. Rather, Defendants' "construction" is a statement of requirements of that would not make sense when inserted into the claim.

83. As to the term "though a data line," Defendants agree that "through" and "data line" do not require construction by repeating them in their proposal. Indeed, these are common technical terms that would be readily understood by a POSITA. (McGraw-Hill Dict.) ("data transmission line: [ELEC] A system of electrical conductors, such as a coaxial cable or pair of wires, used to send information from one place to another or one part of a system to another."). Instead, the only substantive dispute is whether "a data line" is limited to "a ***single*** data line" (as Defendants imply) or whether it is "one or more data lines" (under Solas's construction). Under basic patent law, as well as the intrinsic and extrinsic evidence, Solas's construction is correct.

84. Claim 10 is open-ended and recites: "A display drive apparatus . . . ***comprising***: a gradation signal generation circuit which . . . supplies the gradation current . . . through ***a data line*** . . . ." In these circumstances, it is my opinion that a POSITA would understand that "a" means "one or more."

85. In my opinion, the intrinsic record here supports the conventional rule that "a" means "one or more," and this is not a circumstance where the patentee clearly intended to limit the claim to a single data line. Claim 10 recites a circuit that supplies a current through a data line. A POSITA would understand that current can be supplied through one or more data lines. Further, claim 16 depends from claim 10 and recites "a single data line." If the patentee intended to limit claim 10 to a single data line, it could have said so. Nor in my opinion do the specification or prosecution history support disclaimer (or lexicography). The specification gives examples of one or more data lines, and never expressly limits the system to a single data line.

86. As to the term "through the data line," no further construction is required. The antecedent basis for "the data line" is "a data line" appearing earlier in claim 10.

E. "before" ('137 patent claim 10) / "after" ('137 patent claim 36)

Term	Solas's Proposed Construction	Defendants' Proposed Construction
"before"	plain and ordinary meaning	earlier in time (not at the same time)
"after"	plain and ordinary meaning	later in time (not at the same time)

87. The terms "before" and "after" are common English words and readily understandable to a POSITA. They should receive their plain and ordinary meanings, and no further construction is required. Defendants' proposed constructions of "[earlier/later] in time (not at the same time)" would transform a simple one-word term into a convoluted eight-word phrase with a parenthetical and negative limitation. These constructions are unnecessary, may limit the scope of the terms to be less than their plain and ordinary meaning, and may introduce confusion and ambiguity.

88. For example, Defendants may argue that their constructions require a first process to begin and entirely complete before a second process begins. In other words, Defendants may argue that the two processes cannot be partially overlapping in time, no matter how minute the time overlap

is. I disagree that a POSITA would understand these claim terms in this way. The plain and ordinary meanings of "before" and "after" do not necessarily require that the first process begin and entirely complete before the second process begins.

89. Claim 10 recites in part: "a compensation voltage application circuit which *generates* a compensation voltage for compensating for the threshold voltage of the drive element based on the threshold voltage and *applies* the compensation voltage to the drive element through the data line ***before*** the gradation signal generation circuit *supplies* the gradation current to the display pixel." In view of the claim language and intrinsic evidence, a POSITA would not understand that the generating and applying processes must begin and entire complete before the supplying process. I did not find any disclaimer in the specification or prosecution history that would such a requirement.

90. Claim 36 recites in part: "*supplying*, ***after*** the drive element *holds the voltage*, a gradation current having a current value for allowing the optical element to perform a light emitting operation at a luminance corresponding to a luminance gradation of display data." In view of the claim language and intrinsic evidence, a POSITA would not understand that the supplying process must begin after the holding process begins and completes. I did not find any disclaimer in the specification or prosecution history that would such a requirement.

91. At best, there is a statement in that history that merely indicates that the full plan meaning of "before" or "after" obviously does not cover the situation in which two things happen at the same time—and only happen at the same time:

> By contrast, as recited in independent claim 1 of Application No. 11/888,474 (as amended on July 26, 2010), a gradation voltage compensation circuit generates a compensated gradation voltage by adding a gradation voltage to a compensation voltage, and applies the compensated gradation voltage to the display pixel, wherein the gradation voltage corresponds to a luminance gradation of the display pixel designated by display data, and wherein the compensation voltage is generated by multiplying a specific value detected by a specific value detection circuit with a unit voltage. Thus, in claim 1 of Application No. 11/888,474, the compensation voltage and the gradation voltage are added to be suppled at the same time as a compensated gradation voltage.
>
> It is respectfully submitted, therefore, that claim 1 of Application No. 11/888,474 does not render obvious amended independent claim 1 of the present application, in which the gradation current is supplied as a gradation signal after application of a compensated voltage.
>
> Accordingly, it is respectfully submitted that amended independent claim 1 of the present application is not obvious in view of claim 1 of Application No. 11/888,474.

92. Thus, the above file history is not a disclaimer of claim scope that would normally fall within the plain meaning of the claim term. Rather, it merely conveys that the plain meaning of the added term is not the same as two things only happening at the exact same time—as is the case for two things (gradation voltage and compensation voltage) being added together to create a third thing (compensated gradation voltage), as in the prosecution history excerpt above. This is akin, for example, to saying something like "A must occur before B starts—that is not the same as the prior art, in which A and B only happen at the same time."

VIII. DISPUTED TERMS FOR '891 PATENT

A. "a third thin film transistor which during driving its gate through a driving conductor taps a diode driving current at an output of said first current-driving transistor and supplies a current measuring- and voltage regulating circuit, said current measuring- and voltage regulating circuit providing to the data conductor a voltage signal which is dependent on a current measuring result and a voltage comparison" ('891 patent claims 10, 15, 36, 37, 39)

Solas's Proposed Construction	Defendants' Proposed Construction
Plain and ordinary meaning. The claimed "providing" by the current measuring- and voltage regulating circuit ("said current measuring- and voltage regulating circuit providing to the data conductor a voltage signal which is dependent on a current measuring result and a voltage comparison") is not required to occur during driving of the third thin film transistor's gate.	The claimed "providing" by the current measuring- and voltage regulating circuit ("said current measuring- and voltage regulating circuit providing to the data conductor a voltage signal which is dependent on a current measuring result and a voltage comparison") is required to occur during driving of the third thin film transistor's gate.

93. Defendants do not propose an actual construction for the lengthy claim term "a third thin film transistor . . ." Thus, Defendants appear to agree with Solas that the plain and ordinary meaning should apply. I agree. The claim term is 63 words long, contains terms commonly used in the art, and is readily understandable to a POSITA. It should receive its plain and ordinary meaning and that no further construction is required.

94. The only dispute is between the parties whether the claimed "providing" by the current measuring- and voltage regulating circuit ("said current measuring- and voltage regulating circuit providing to the data conductor a voltage signal which is dependent on a current measuring result and a voltage comparison") is required to occur during driving of the third thin film transistor's gate. I agree with Solas that the claimed "providing" is ***not*** required to occur during driving of the third thin film transistor's gate. A POSITA would understand that the claimed "providing" is not required to occur in view of the claim language and intrinsic evidence. There is no lexicography that compels such extreme narrowing from the plain meaning. And Defendants have not pointed

to—and cannot point to—any clear disclaimer of its invention from the prior art to warrant the narrowing it seeks, either.

95. A POSITA would understand that the first portion of the claim term before the comma describes two functions of the thin film transistor that are performed during driving of the transistor's gate: (1) "taps a diode driving current" and (2) "supplies a current measuring- and voltage regulating circuit." A POSITA would understand that the preposition "during" modifies the verbs "taps" and "supplies" in this claim language:

> "***a third thin film transistor*** which ***during driving*** its gate through a driving conductor ***taps a diode driving current*** at an output of said first current-driving transistor and ***supplies a current measuring- and voltage regulating circuit***, "

96. A POSITA would not understand that the proposition "during" modifies the later "providing" claim language because that language is separated by a comma and constitutes a separate clause and limitation:

> "***a third thin film transistor*** which ***during driving*** its gate through a driving conductor ***taps a diode driving current*** at an output of said first current-driving transistor and ***supplies a current measuring- and voltage regulating circuit, said current measuring- and voltage regulating circuit providing*** to the data conductor a voltage signal which is dependent on a current measuring result and a voltage comparison"

Indeed, I note that Defendant LG Display submitted an IPR petition on the '891 patent that described the disputed term as two separate claim limitations: limitation [1e.1] for the language preceding the comma and limitation [1e.2] for the language after the comma. *See* Solas's Extrinsic Evidence Disclosure, Ex. G (Petition and Declaration in IPR2020-00177) at 45, 48.

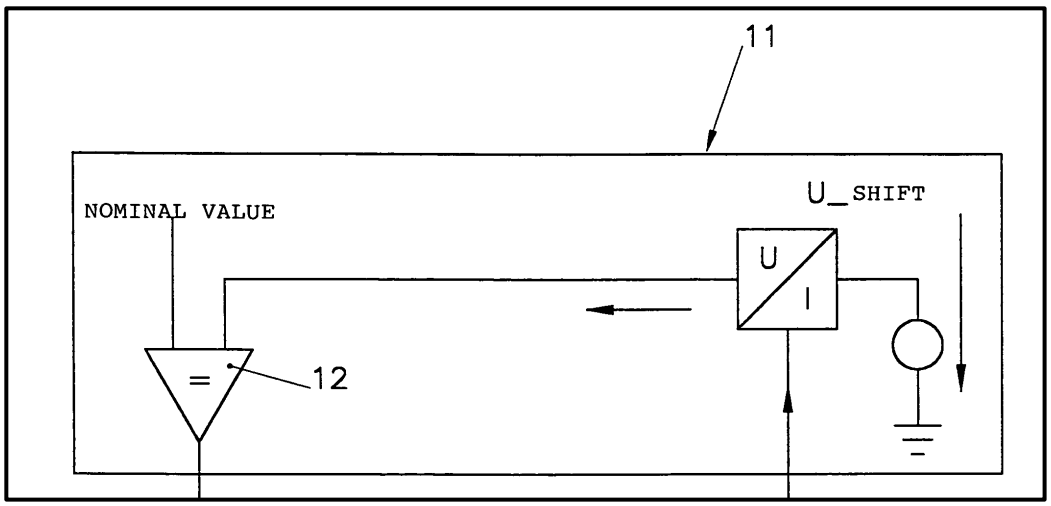
97. Further, a POSITA would understand that the proposition "during" modifies the two functions of the *third thin film transistor*. It does not modify the claimed "providing," which is performed by the current measuring- and voltage regulating circuit.

98. The specification of the ’891 patent is consistent with the claim language and supports my understanding. For example, it states: “the circuit has a third film transistor T3. During driving of its gate, it taps the driving current of the LED element directly at the source electrode of the thin film transistor T1 and supplies it to a current measuring- and voltage regulating circuit 11.” ’891 patent at 3:8–12. This describes the tapping and supplying functions of the third transistor that occur during driving of the transistor’s gate. It does not require the claimed “providing” by the current measuring- and voltage regulating circuit to occur during driving of the transistor’s gate. I did not find any disclaimer in the specification or prosecution history that would support Defendants’ requirement and disagree there is disclaimer. Defendants have not identified any portions of the specification or prosecution history that would support their proposal. To the extent Defendants identify such portions and argue disclaimer, I reserve the right to respond.

B. “current measuring” (’891 patent claims 1, 3)

Solas’s Proposed Construction	Defendants’ Proposed Construction
plain and ordinary meaning	measuring actual current (not voltage)

99. Just as with Defendants’ construction for “gradation current” in the ’137 patent discussed above, Defendants’ proposal for this term improperly inserts a negative limitation without support in the specification or intrinsic record. This term is used in the claims as a unit-qualifier, describing a claimed structural circuit: current measuring- and voltage regulating circuit:



The portion of the '891 patent figure shows a current ("I") entering a box labeled "U/I" and a voltage exiting. (The symbol "U" is sometime used for voltage, as evidenced by the patent's discussion of "the voltage source U shift." ('891 patent at 3:25–26.)) The voltage "U" is then compared to a "nominal value" voltage in a "voltage comparison" in the "comparator 12." (*Id.* at 2:7, 3:17–18.) *See* Ex. G., Declaration of Miltiadis Hatalis, Ph.D. in support of IPR, ¶ 76.

100. In my opinion, Defendants' proposed construction does not actually define the term. Their proposal is to merely repeat all the words of the disputed term itself, "current" and "measuring," into the construction verbatim, but then also add a negative limitation.

101. In merely repeating all the same words of the disputed term, it is clear that both sides agree that no word in the actual disputed claim term requires further construction. Instead, the disputed term obviously has a plain meaning to a POSITA.

102. Defendants do not import just any kind of limitations around the words of the actually disputed claim term they import negative limitations. I can identify no lexicography that compels such a narrowing from the plain meaning. And Defendants have not pointed to—and I have not identified—any clear disclaimer of its invention from the prior art to warrant the narrowing Defendants seek, either.

103. Instead of helping the jury get a sense of some term for which a POSITA would not already have a clear understanding, Defendants' proposal only adds more words and suggests to the fact-finder that current measurement that also involve the inextricable intertwined concept of voltage are outside the scope of the '891 patent claims. I explain that relationship in several other places n this declaration so there is no need to repeat it again here.

C. "wherein all above mentioned elements of the driving circuit are located at a same side of said light emitting diode" ('891 patent claim 3)

Solas's Proposed Construction	Defendants' Proposed Construction
wherein all above mentioned elements of the driving circuit are electrically connected to and physically located on the same side of the layers of said light emitting diode	wherein all above mentioned elements of the driving circuit are electrically connected to the anode or cathode of said light emitting diode

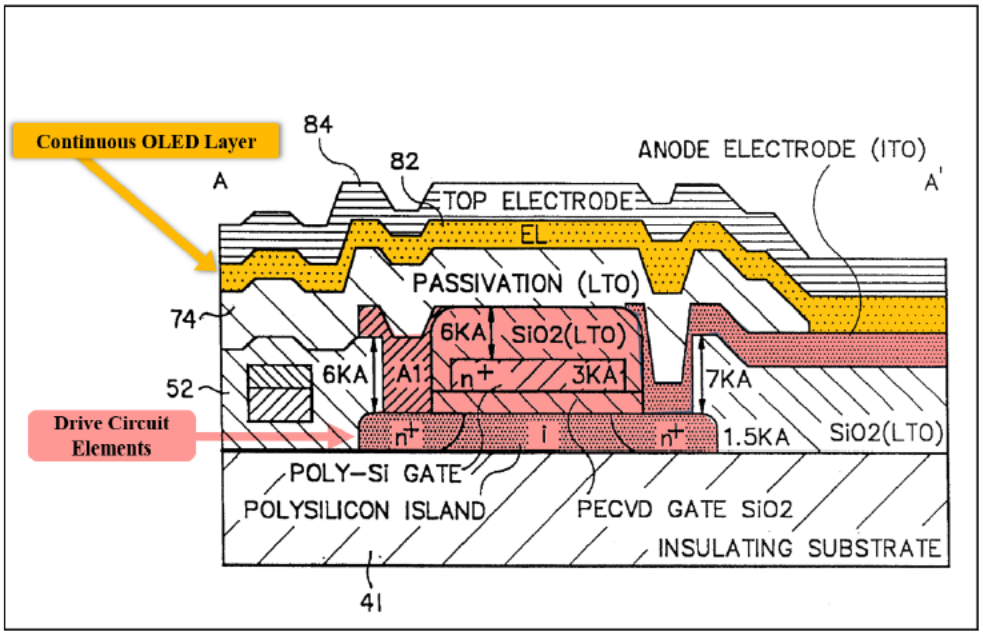
104. A POSITA would the term to mean "physically located on the same side of the layers of said light emitting diode" in view of the claim language, intrinsic evidence, and extrinsic evidence. A driving circuit as recited in the '891 patent is manufactured as one or more layers. Further, organic light-emitting diodes include "one or more layers of organic material [] sandwiched between two electrodes," i.e., an anode a cathode. U.S. Patent App. Pub. 2002/0101172 at [0005] (cited by '891 patent at 1:32–36). Thus, "located on the same side" means that all the drive circuit elements are located on the same physical side of the layers of the diode, i.e., above or beneath the organic layer and on the same side as the anode or cathode.

105. The plain meaning of the actual claim term "located at" refers to physical location. For example, the English word "locate" means "to set or establish in a particular spot." This is consistent with the plain meaning of "located at a same side of said light emitting diode" in the context of the '891 patent. A POSITA would understand that drive circuit elements and diodes are physical semiconductor components that are arranged in physical locations during manufacture.

Indeed, the claim language references physical components by mentioning "contacts" of the "semiconductor material of the diode." Solas's proposal is also consistent with the remaining claim language: "so that no contacts must be guided through a semiconductor material of the diode." A POSITA would understand that if all drive circuit elements are physically located on the same side of the layers of the diode, e.g., beneath or above the organic layer, then no contacts must be guided through the organic layer, i.e., "semiconductor material of the diode."

106. Defendants' proposal is incomplete because A POSITA would understand that electrical connection and physical location are different concepts. Whereas electrical connections of a driving circuit are depicted in a circuit diagram (such as in the figure of the '891 patent), a circuit diagram does not depict the physical locations of the driving circuit elements relative to the diode.

107. Indeed, Defendant LG Display ("LGD") filed an IPR petition on the '891 patent confirming that electrical connection and physical location are different concepts. LGD provided the following figure in discussing the "located at a same side" limitation (LGD Pet. at 64):



LGD argued that this shows that "the layers comprising the driving circuit can *all be located on* ***the same physical side*** *of the OEL layer (in the figure above, the bottom side*." *Id.* (emphasis added). LGD further argued that a reference's disclosure its drive elements electrically connected to one side of the diode "would allow ***placing those drive elements on the same side during manufacture*** and that no contacts guided through the diode's semiconductor material would be necessary." *Id.* at 64–65 (emphasis added).

108. Thus, LGD agreed electrical connection and physical location are different concepts. I further agree that a claim term "located at a same side of said light emitting diode" is satisfied if the layers comprising the driving circuit located on the same physical side of the OEL layer, which is consistent with Solas's proposed construction. I further agree that "located at a same side" refers to where the driving circuit elements are physically placed during manufacture.

109. Defendants' construction is wrong because "located at the same side" of is not limited to or coextensive with "electrically connected to the same side." I did not find any lexicography or disclaimer in the specification or prosecution history that would redefine "located at" to mean "electrically connected to."

110. For example, a POSITA would not view the Applicant's statements during prosecution to operate as lexicography or clear and unmistakable disclaimer. The Applicant distinguished the pixel matrix and the measuring circuit of the Inukai and Bu references because they "are located on (respectively connected to) the anode and the cathode side of the OLED device." '891 FH, 152–53. A POSITA would not understand the parenthetical to redefine "located on" to mean "respectively connected to" but rather as an additional requirement. This is confirmed by the Applicant's statement in the same Office Action that claim 3 "is ***not just about*** the physical layers, but about the circuit elements." *Id.* (emphasis added). A POSITA would understand this statement

to mean that claim imposes requirements both about the physical layers of the driving circuit and the electrical connections of the circuit. Further, the Applicant's statement that "the above mentioned interrelations between a circuit structure and a physical layering are trivial" (*id.* at 153–54) does not operate as lexicography or disclaimer.

IX. DISPUTED TERMS FOR '068 PATENT

A. "formed on said plurality of supply lines along said plurality of supply lines" ('068 patent claim 1)

"connected to said plurality of supply lines along said plurality of supply lines" ('068 patent claim 13)

Term	Solas's Proposed Construction	Defendants' Proposed Construction
"formed on said plurality of supply lines along said plurality of supply lines"	formed on said plurality of supply lines over the length or direction of said plurality of supply lines	formed on said plurality of supply lines over the length of said plurality of supply lines
"connected to said plurality of supply lines along said plurality of supply lines"	connected to said plurality of supply lines over the length or direction of said plurality of supply lines	connected to said plurality of supply lines over the length of said plurality of supply lines

111. The '068 patent claims recite "a plurality of feed interconnections" which are "formed on" (claim 1) or "connected to" (claim 13) "said plurality of supply lines along said plurality of supply lines." As shown above, the parties' sole dispute concerns the meaning of "along." Defendants' construction is that along means "over the length of," whereas Solas's construction is that along means "over the length *or direction* of." The plain meaning of the claim language, as well as the intrinsic and extrinsic evidence, show that Solas is correct.

112. The plain meaning of "along" is over the length or direction of. Dictionaries define along in precisely this way. *See* Ex. E (Merriam-Webster Dictionary) ("along: 1: in a line matching ***the length or direction of*** // walking *along* the river; *also*: at a point or points on // a house *along* the

river"); Ex. F (Dictionary.com) ("along: 1 through, on, beside, over, ***or parallel to the length or direction of***; from one end to the other of: *to walk along a highway*."). To say that "I walked along the Mississippi River" does not mean that I walked over the length of the Mississippi River. Rather, it means that I walked in the direction of the Mississippi River over some portion of its length.

113. The claim language uses "along" consistent with this plain meaning. The claims recite a plurality of feed interconnections "formed on" or "connected to" a plurality of supply lines "along" the plurality of supply lines. A POSITA would understand that the feed interconnections are formed on or connected to the supply lines over the direction of the supply lines. The claims do not require the feed interconnections to be formed or connected over the length of the supply lines—nor require the feed interconnections and supply lines to be the same length. Indeed, based the parties' proposals, the parties agree that feed interconnections are "conductive structures in a layer or layers" and that supply lines are "conductive lines." A POSITA would not understand that conductive structures need to be formed on or connected to conductive lines over the length of those lines. There is no lexicography that compels such extreme narrowing from the plain meaning. And Defendants have not pointed to—and cannot point to—any clear disclaimer of its invention from the prior art to warrant the narrowing it seeks, either.

114. The specification also supports Solas's construction. In describing an example of the overall arrangement of the display panel, it states that the feed interconnections and its common connections are provided "***in parallel to***" the supply lines. *See* '068 patent at 6:26 ("The feed interconnections 90 *are provided in parallel to the supply lines* Z_1 to Z_m when viewed from the upper side. The common interconnections 91 *are provided in parallel to the signal* lines Y_1 to Y_n when viewed from the upper side."); *see also id.* at 23:1–6. This shows that the feed

interconnections are formed on or connected to the supply lines at particular locations and that those locations are "parallel to" (in the direction of) the supply lines.

115. Defendants' constructions are incorrect because they are not the plain meaning and because there is no lexicography or disclaimer that requires them. For example, the specification and prosecution history do not redefine "along" to mean "over the length of." Nor do they require the feed interconnections to be formed on or connected to the supply lines over the length of the supply lines.

B. "patterned" ('068 patent claims 1, 13)

Solas's Proposed Construction	Defendants' Proposed Construction
formed in one or more layers	formed in a single layer

116. Defendants separately identified the individual word "patterned" as one that supposedly requires construction in addition to identify the two-word, actually claimed phrase, "patterned together," as a separate term that requires construction. Joint Revised List of Terms/Constructions, p. 4. But notably, the word "patterned" does not exist in the claims by itself. Rather, it only shows up as in the two-word claimed phrase "patterned together." Nevertheless, because Defendants split up the term from its two-word phrasing in the actual claim, Solas proposed a construction that crystallizes the dispute and why Defendants must be wrong in their construction of it.

117. As with all terms, I provide the below additional explanation in addition to the relevant explanations I provide in my patent and technology background sections.

118. The '068 claims describe driving circuit elements "patterned" together on a substrate. *See* '068 patent, cls. 1, 13. The parties agree that "patterned" must convey, at a minimum, the end result of after those circuit elements are "formed." The only dispute is whether patterning requires

forming "in a ***single layer.***" It does not. The plain meaning of "patterned" is not limited to a single layer. Because there is no lexicography or disclaimer, Defendants' construction should be rejected.

119. "Patterned" is a known term of art with a plain meaning to a POSITA. It refers to forming or shaping of semiconductor regions and components using a designed photolithographic process, namely, photolithographic exposure and etching. patent at 11:4–6 ("pixel electrodes 20a are formed, using photolithography and etching, by patterning a conductive film"). This process can be applied to a single layer or to multiple layers, such as a stack. A POSITA would not understand the usage of the term to be limited to designs in a single layer only. This is confirmed by other references in the art, which commonly describe "patterning" multiple layers. Ex. I ('652 patent) at 1:57–60 ("In the forming process, *the layers 3 through 5 and 10* . . . are patterned by dry etching or like methods); Ex. J ('317 patent) at 4:64–67 ("By a photolithographic and etching technique, the films 25', 22', and 21' are now patterned to form the [three-layer] gate structure 25,22,21 of FIG. 5."). Thus, a POSITA would understand patterned means "formed in one or more layers" and is not limited to a single layer. I see no lexicography that compels such extreme narrowing from the plain meaning.

120. The '068 patent uses "patterned" consistent with this plain meaning. As shown in Fig. 5 below, the specification describes a "drain layer" structure that includes drain 22d and source 22c, in which each can be "a layered structure including ***two or more layers***."'068 patent at 9:44–49, 8:47–51. Thus, the drain layer is a stack of multiple layers. The specification teaches that the drain layer is patterned, including with photolithography and etching. *See id.* at 9:50–53 ("the drain layer is ***patterned*** . . . the ***patterned*** drain layer is superposed"), 14:46–48 ("The drain layer is sequentially subjected to photolithography and etching to ***pattern*** the drains 21d, 22d, and 23d, the

sources 21s, 22s, and 23s[.]") This confirms that "patterning"—as used in the '068 patent—includes forming one or more layers and is not limited to a single layer.

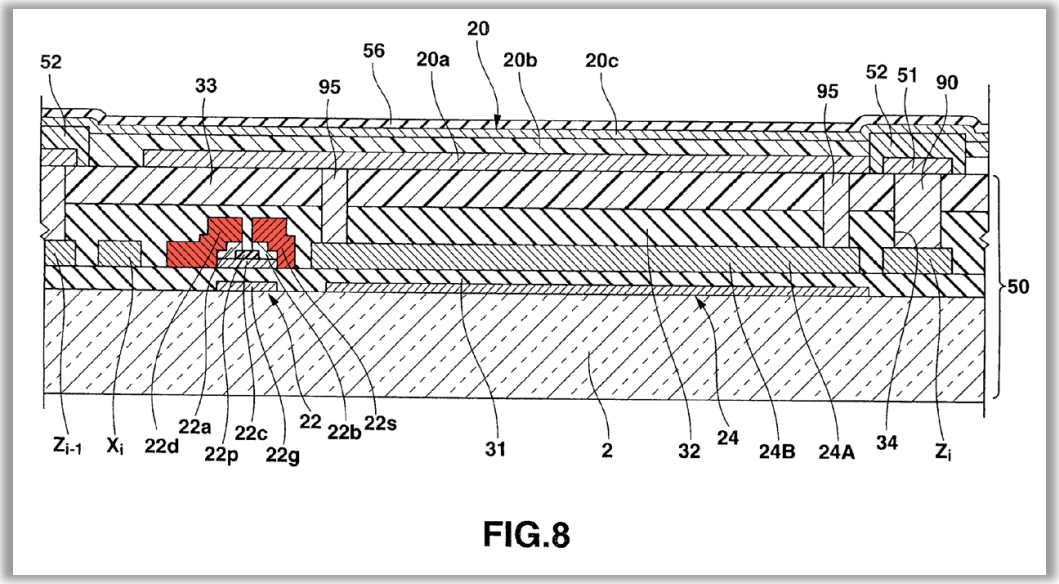


FIG.8

C. "patterned together" ('068 patent claims 1, 13)

Solas's Proposed Construction	Defendants' Proposed Construction
patterned to fit together	patterned at the same time

121. As with many or all of the terms in this declaration, I provide the following in addition to the explanations that I include in my technology and patent background sections.

122. The parties dispute centers on the meaning of "together." Defendants interpret patterned together to mean "patterned ***at the same time***," whereas Solas interprets it to mean "patterned to fit together." Thus, it appears that the parties dispute whether "together" reflects spatial relationship (in Solas's construction) or a temporal relationship (in Defendants' construction). Defendants also require the patterning to be simultaneous.

123. The plain meaning of "together" is into a coherent structure or integrated whole. In this regard, a POSITA's understanding would be consistent with various non-technical definitions of

the term as well. *See* Ex. E (Merriam-Webster Dictionary) ("together: 4b: in or into a unified or coherent structure or an integrated whole"); Ex. F (Dictionary.com) ("together: 2: into or in union, proximity, contact, or collision, as two or more things: *to sew things together*). The claims uses "together" consistent with this plain meaning. A POSITA would understand "patterned together" to mean that drive circuit elements formed to fit together.

124. The '068 specification uses "patterned together" in the same way. It makes clear that "patterned together" means the spatial sense of patterned to fit together, not the temporal sense of patterned at the same time. For example, the specification describes "conductive lines 51 patterned together *with* the pixel electrodes 20a *by etching a conductive film as the* ***prospective*** *pixel electrodes 20a."* '068 patent at 11:11–14. Etching a film for "prospective" (future) electrodes ensures that the conductive lines will fit together when the actual electrodes are formed. This confirms that "patterned together"—as used in this patent—does not refer to the *timing* of when those elements are formed, but rather the *spatial* relationship between the conductive lines and pixel electrodes,

125. This understanding is confirmed by other patents in the art, including '772 patent cited in Defendants' extrinsic evidence disclosure. The '772 patent describes "a first reflective electrode 294 will be *patterned together*"

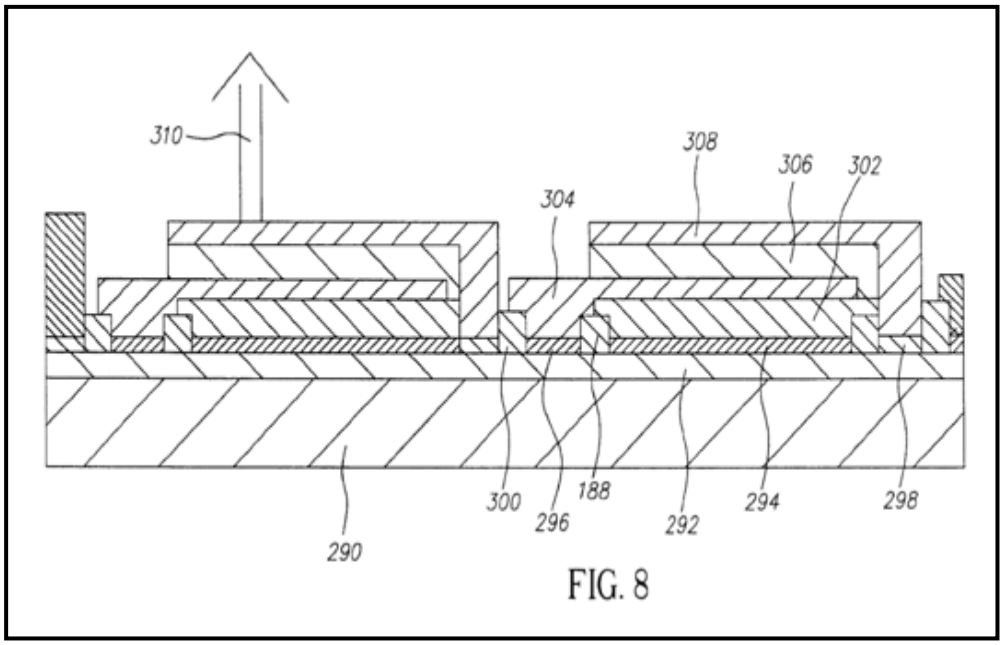


FIG. 8

126. In this teaching, the patent states that a "first reflective electrode ***294*** will be *patterned together* with first ***296*** and second ***298*** connectors…" It is clear that ***294*** and ***298*** are not stacked one upon the other. It is also clear that ***294*** and ***298*** appear as two distinct, laterally separated layers. As such, they cannot be patterned in one photolithographic step. Layers ***294*** and ***296*** were patterned at different times with different pattern masks.

127. Defendants' construction is incorrect because a POSITA would not understand "together" to mean "at the same time" in the context of the '068 patent. Nor is there any lexicography or disclaimer that requires this construction. To the contrary, the '068 patent expressly teaches patterning a "drain layer" composed of multiple layers. A POSITA would know that multiple layers cannot be "formed at the same time." Finally, even if "patterned together" referred to timing, it should include sequential as well as simultaneous patterning.

128. I can identify no lexicography that compels such a narrowing from the plain meaning. And Defendants have not pointed to—and I have not identified—any clear disclaimer of its invention from the prior art to warrant the narrowing it seeks, either.

D. "signal lines" ('068 patent claims 1, 13)

Solas's Proposed Construction	Defendants' Proposed Construction
conductive lines supplying signals	conductive lines supplying a value corresponding to a luminance level

129. Defendants' proposed construction improperly limits the claims by importing into the term features of the background art or preferred embodiments from the specification. The parties agree that the "signal lines" are conductive lines and that they supply something. Where the parties depart is in what that *something* is that they must supply.

130. Solas's construction correctly follows the plain meaning of the term, by requiring that the signal lines supply "signals." Defendants propose a more specific construction, requiring that they supply "a value corresponding to a luminance level." But nothing in the claims mentions "luminance" or suggests that the invention should be limited to supplying luminance signals. In my opinion, Defendants' construction is not commensurate with the plain meaning of the term. Nothing in the specification or file history provides a special definition of "signal lines" or a disclaimer that supports Defendants' construction.

131. Indeed, the only time that the specification even uses the word "luminance" in the same paragraph as "signal line" is in the background "description of the related art," where it describes a "conventional" prior art display and says "a voltage of level representing the luminance is applied to the gate of the driving transistor through a signal line." ('068 patent at 1:38–40.) As understood by a POSITA, this is not a definition of "signal line," and it does not indicate that "signal line" has a specialized meaning in the patent.

E. "feed interconnections" ('068 patent claims 1, 10, 12, 13, 17)

Solas's Proposed Construction	Defendants' Proposed Construction
conductive structures in a layer or layers that provide connections to a source that supplies voltage and/or current	conductive structures in a layer or layers different from the gates, sources and drains that provide connections to a source that supplies voltage and/or current

132. The plain meaning of "interconnections" in the context of the '068 patent is a conductive structure in a layer or layers that provides electrical connections between two circuit elements. As the overlap between the two competing constructions makes clear, the parties essentially agree on this point. The parties' competing constructions also confirm agreement that the "feed interconnections" species of connections provides connections to "a source that supplies voltage and/or current." This is the plain and ordinary meaning of the disputed term.

133. The only remaining dispute concerns Defendants' importation, beyond the plain meaning of the disputed term, that the conductive structures are in "layer or layers" that are "***different from*** the gates, sources and drains." There is inconsistent with the plain meaning of the term. There is no lexicography that compels such extreme narrowing from the plain meaning. And Defendants have not pointed to—and my analysis has not revealed—any clear disclaimer of its invention from the prior art to warrant the narrowing it seeks, either.

X. CONCLUSION

I declare under penalty of perjury that the foregoing is true and correct.

Executed March 13, 2020 in San Ramon, California.

By: 

Richard A. Flasck